What is claimed is:

1. A data processor for processing data comprising:

an input port for receiving packets of data;

at least a port for communication with each of a plurality of processors;

a first processor in communication with the at least a port and for processing received data to provide a header including a list of processes to perform on the packet of data and an ordering thereof, the header stored within a packet of data to which the header relates;

a buffer for storing data received from the at least a port ;

a buffer controller for determining based on the header within a packet a next processor of the plurality of processors to process said data packet and for providing said data packet to the at least a port for provision to the next processor.

2. A data processor for processing data as defined in claim 1 wherein first processor includes means for providing executable code to the next processor, the executable code for being executed to process an associated packet.

3. A data processor for processing data as defined in claim 1 wherein first processor includes means for providing an indication of executable code to provide to the next processor, the executable code for being executed to process an associated packet.

4. A data processor for processing data as defined in claim 1 wherein buffer controller is for determining the next processor from a plurality of available processors each of which is a possible next processor.

5. A data processor for processing data as defined in claim 1 further comprising the plurality of processors.

6. A data processor for processing data as defined in claim 5 wherein the plurality of processors is a plurality of special purpose processors.

7. A data processor for processing data as defined in claim 6 wherein the plurality of special purpose processors includes cryptographic processors having secret keys stored therein and inaccessible from outside the cryptographic processor device.

8. A data processor for processing data as defined in claim 7 wherein the plurality of special purpose processors includes a plurality of processors for performing aspects of network security protocol processing in order to support at least a network security protocol.

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9. A data processor for processing data comprising:

a buffer for storing data;

a plurality of special purpose processors, each for processing data from within the buffer;

a buffer controller in communication with each special purpose processor, for determining a next processor of the special purpose processors to process the data, and for providing the data to the determined next processor.

10. A data processor for processing data as defined in claim 9 wherein the plurality of special purpose processors includes at least a server processor for formatting data into a data structure including a header having a list of processes to perform on the data and an ordering thereof.

11. A data processor for processing data as defined in claim 10 wherein the buffer controller is for determining a next process in dependence upon the list of processes to perform on the data and the ordering thereof.

12. A data processor for processing a packet of data comprising:

an addressing network;

a plurality of special purpose processors, each for processing data received via the addressing network and for providing processed data to the addressing network, the addressing network interconnecting the plurality of special purpose processors;

a first processor for providing data for use in directing a packet of data through the addressing network to a plurality of processors one after another in a predetermined order, the data associated with the packet, wherein different packets are provided with different data for directing them differently through the addressing network and wherein each special purpose processor is for performing a function absent knowledge of the overall high level packet processing operation.

13. A data processor for processing a packet of data as defined in claim 12 wherein each processor is for receiving executable instructions and for executing same, the executable instructions provided to the processor along a different data path than the data packet.

14. A data processor for processing a packet of data as defined in claim 12 wherein each processor is for receiving executable instructions and for executing same, the executable instructions provided to the processor along a same data path than the data packet.

15. A method for processing stream data comprising:

receiving stream data including packets of data at an input port;

processing received data packets to provide for each a header including a list of processes to perform on the packet and an ordering thereof, the header stored within the packet to which the header relates;

providing the packet with the associated header to a buffer for storage;

for each packet within the buffer:

determining based on the header within the packet a next processor to process the packet;

providing the packet to the determined next processor for processing, and

receiving the processed packet from the processor and storing it in the buffer, the stored packet including one of an indication that processing by the next processor is complete and that no processing by the next processor is required; and,

when no further processes are indicated in a header of a packet, providing the packet to an output port.

16. A method for processing stream data as defined in claim 15 wherein prior to providing the packet to the output port, the header information is stripped therefrom.

17. A method for processing stream data as defined in claim 16 wherein the method is implemented within a single integrated device.

18. A method for processing stream data as defined in claim 16 wherein the method is implemented within a single integrated device absent at least some of the next processors and wherein the at least some next processors are in communication with the integrated device.

19. A method for processing stream data as defined in claim 18 wherein the integrated device includes an input port, an output port, a server processor for providing the header information and a data buffer for storing packet data and for routing the packet data between next processors.

20. A method for processing stream data as defined in claim 19 wherein the server processor is programmable.

21. A method for processing stream data as defined in claim 19 wherein the input port and the output port include data elements for ingress and outgress processing respectively.

22. An architecture for processing data comprising:

a first processing element for receiving data and for formatting the data with a list of processes selected from available processes and an ordering thereof, the list of processes for being performed on the data;

further processors for performing at least one process from the available processes; and,

a routing memory for providing data to processors for performing the processes according to the ordering of the listed processes.

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23. An architecture for processing data according to claim 22 wherein the routing memory comprises a packet buffer memory for buffering packets and a processor for determining an appropriate processor for processing the formatted data and for providing the data to said processor.

24. An architecture for processing data according to claim 22 wherein the routing memory comprises an address switching network for routing a packet between processors in a predetermined order according to the list of processes and the ordering thereof wherein the address switching network is dynamic allowing a packet to be routed between further processors in accordance with any of a variety of process lists and orders.

25. An architecture for processing data according to claim 22 wherein some of the further processors are dedicated single function processors for processing the data.

26. An architecture for processing data according to claim 25 wherein a majority of the further processors are dedicated single function processors for processing the data.

27. An architecture for processing data according to claim 26 wherein a majority of the further processors are processor modules for interfacing with the routing memory.

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